B1 Cont'd

(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential.

Please add claims 10-18 as follows:

10. (New) The integrated circuit of claim 1, wherein the first bipolar transistor couples the isolation region to the reference potential input when the substrate potential is higher than the reference potential.

11. (New) The integrated circuit of claim 1, wherein the first bipolar transistor is off when the substrate potential is less than the reference potential.

12. (New) The integrated circuit of claim 1, wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

B2

13. (New) The integrated circuit of claim 1, wherein the collector of the first bipolar transistor is directly connected to the reference potential input.

Sub C1

14. (New) The integrated circuit of claim 1, wherein the emitter of the second bipolar transistor is directly connected to the substrate.

15. (New) The semiconductor device of claim 7, wherein the first bipolar transistor couples the isolation region to the reference potential input when the substrate potential is higher than the reference potential.

16. (New) The semiconductor device of claim 7, wherein the first bipolar transistor is off when the substrate potential is less than the reference potential.

17. (New) The semiconductor device of claim 7, wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

B2 Concl'd

18. (New) The semiconductor device of claim 7, wherein the collector of the first bipolar transistor is directly connected to the reference potential input.